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Universal Liquid Metal Interconnects for Next-Generation Glass Packaging

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Received: 27 January 2026 | **Revised:** 20 March 2026 | **Accepted:** 30 March 2026

Keywords: 3D printing | anisotropic conductive adhesives | glass interposers | liquid metals | through-glass vias

ABSTRACT

Advances in 2.5D heterogeneous integration demand interconnect technologies that combine fine pitch, thermal and mechanical reliability, and scalable manufacturability on glass interposers. Here, we introduce a versatile platform that exploits the fluidic and electrical properties of gallium-based liquid metal (LM), leveraging LM's larger skin depth than copper to mitigate high-frequency skin-effect losses. First, vacuum-assisted capillary infiltration forms conformal, void-free LM-filled through-glass vias, eliminating seed-layer deposition and electroplating while lowering thermal budget. Second, 3D direct microprinting of LM writes interconnects with 5 μm resolution, enabling dense chip-to-interposer fan-out beyond wire-bonding limits. Third, an LM-based anisotropic conductive adhesive (LM-ACA) provides vertical electrical interconnection and mechanical adhesion at room temperature and low pressure, reducing assembly complexity and supporting panel-scale integration. Integrating these technologies, we demonstrate stable operation, including real-time sensing, processor operation, and chip-to-chip communication, establishing LM as a fine-pitch, thermally resilient, and scalable interconnect medium for glass-based 2.5D packaging.

1 | Introduction

As demand from artificial intelligence and high-performance computing grows and successive high-bandwidth memory generations continue to advance, simply increasing vertical stacking no longer overcomes thermal, yield, and cost constraints [1, 2]. At the same time, as device-level scaling becomes constrained by Moore's law, further improvements in performance and efficiency now rely on system-level integration. In this context, chiplet-based integration, rather than relying on monolithic large-area dies or complex 3D stacking, improves effective yield, mitigates reticle-size limitations, and reduces manufacturing cost [3]. 2.5D integration, as a representative form of chiplet-based integration, has emerged as a leading approach for system-level scaling through heterogeneous integration, by colocating multiple chiplets and memory dies on a high-density interposer with wide I/O interfaces and short interconnect paths [4]. In this architecture, the interposer acts as an intermediary substrate between individual chips and the package or printed circuit board (PCB). It provides fan-out for die-to-die and die-to-package connections, while supporting integrated redistribution layers (RDLs) and power delivery networks [5].

Inhea Jeong and Wonjung Park contributed equally to this work.

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The rapid advance of high-frequency electronic packaging has driven a need for vertical interconnects that minimize signal loss at microwave and mm-wave frequencies. Through-glass vias (TGVs) in glass interposers have emerged as a promising solution for next-generation high-density integration because glass offers ultralow dielectric loss and high electrical resistivity, enabling significantly lower RF insertion loss than silicon-based interposers [6]. TGV-based glass interposer manufacturing has advanced rapidly across via drilling and postdrill cleaning, seed-layer deposition and electroplated metallization, and RDL build-up [7]. In particular, TGV technology has been successfully used to realize high-Q inductors and capacitors for RF front-ends, leveraging glass's insulating properties to achieve quality factors unachievable on silicon [8]. However, current TGV fabrication still depends on copper (Cu) seed-layer deposition followed by electroplating, and as via aspect ratios increase, maintaining uniform seed coverage and stable plating becomes challenging, often resulting in void defects that impair electrical continuity and resistance uniformity [9, 10]. Furthermore, the coefficient of thermal expansion (CTE) mismatch between Cu and glass remains a critical issue, which can cause irreversible damage such as cracking, interfacial delamination, and Cu protrusion, ultimately compromising long-term reliability [11, 12]. In addition to these mechanical concerns, electrical losses also become significant. Cu is the conventional choice due to its excellent DC conductivity, but at high frequencies the effective conductivity of Cu interconnects deteriorates because of the skin effect and surface roughness-induced scattering [13]. As current at MHz frequencies concentrates near the conductor surface, any surface roughness or grain boundary irregularities in plated Cu can substantially increase resistive loss and frequency-dependent impedance [14]. Indeed, recent studies on Cu thin films and coatings have shown that their RF conductivity can deviate markedly from the bulk value, with rough or composite Cu layers exhibiting higher loss or anomalous frequency dispersion compared to smooth Cu surfaces. These findings underscore that simply using a high-DC-conductivity metal like Cu does not guarantee low loss in the high-frequency regime, as conductor surface quality becomes a dominant factor [15]. Collectively, these coupled process limitations, CTE mismatch, and high-frequency losses impose fundamental constraints on the scalability and long-term reliability of Cu-based TGV/RDL architecture on glass.

Beyond interposer fabrication, package-level assembly that connects chips, the interposer, and the PCB imposes additional constraints. Solder flip-chip, thermocompression, and Cu–Cu hybrid bonding require elevated thermal and pressure budgets, along with stringent planarity and surface cleanliness, which increase process complexity, limit fine-pitch scalability and panel-level throughput [2, 16]. These approaches inherently rely on solid-state metallic bonding at high temperature and pressure, which amplifies mechanical stress at chip–interposer interfaces under thermal loading during active operation. As a result, mismatches in CTE among materials can induce warpage, interfacial cracking, or delamination, ultimately compromising electrical integrity and system reliability [10]. Meanwhile, wire bonding typically operates at pitches of twenty micrometers or larger, limiting high-density integration and complicates routing for complex, multichip configurations. Therefore, to fully exploit the advantages of glass interposers, an interconnect that combines ultrafine pitch capability, robust thermal reliability under low-temperature and low-pressure conditions, and true panel-level scalability within a wide process window is required.

Here, to address this challenge, we present an liquid metal (LM)-based interconnect platform using eutectic gallium–indium (EGaIn) to achieve via metallization, fine-pitch 3D bonding, and an LM-based anisotropic conductive adhesive (LM-ACA) assembly. First, LM's fluid injectability enables conformal, void-free metallization through simple vacuum-assisted capillary infiltration (VACI). At high frequencies, EGaIn's larger skin depth allows current to distribute through more of the via cross section, reducing the resistive penalty of its lower conductivity, while the absence of plating interfaces or grain boundaries eliminates additional scattering pathways [17, 18]. Using an LM that does not store static shear suppresses shear accumulation under temperature excursions, and a stiffness-optimized RDL that carries the hydrostatic load of the LM-filled TGVs confines deformation to a reversible elastic regime, ensuring thermomechanical and electrical reliability. Second, 3D microprinting of LM directly writes interconnects with a resolution of five micrometers, enabling dense chip-to-interposer fan-out on glass and surpassing the practical pitch limitations of wire bonding. Third, an LM-ACA enables vertical electrical interconnection and mechanical adhesion without requiring elevated temperature and pressure, thereby reducing assembly complexity and enabling reliable panel-scale integration. Together, these advances establish LM as a package-level interconnect medium that combines ultrafine pitch, robust thermal reliability, and panel-scale manufacturability, advancing a unified platform for glass-based 2.5D packaging at high density and high frequency.

2 | Results

2.1 | Liquid Metal in Semiconductor Packaging and Interposer Filling

Figure 1a schematically illustrates three complementary roles of LMs in 2.5D glass interposer packaging: (i) LM-filled TGVs for interposer metallization, (ii) 3D direct-printed LM interconnects for chip-to-chip and chip-to-interposer wiring, and (iii) LM-ACA that enable low-temperature, low-pressure assembly between chip and interposer, as well as between interposer and PCB. Figure 1b highlights LM-filled TGVs, contrasting them with conventional Cu-filled TGVs that require seed-layer deposition and electroplating [19]. In Cu-filled TGVs, higher aspect ratios hinder uniform seeding, cause void formation that degrades electrical uniformity, and make fabrication more complex and time-consuming. To address these limitations, we demonstrate room-temperature VACI of LM. This approach eliminates both seed-layer deposition and electroplating, simplifies fabrication, shortens cycle time, and enables conformal, void-free metallization even at high aspect ratios. Thermomechanically, Cu-filled TGVs suffer from a large CTE mismatch between glass and Cu. Combined with Cu's high modulus and yield strength, this mismatch induces cycle-to-cycle interfacial shear accumulation, leading to progressive and irreversible damage such as delamination, cracking, and protrusion. By contrast, in LM-filled TGVs, the LM does not sustain static shear stress. Thermal excursions therefore manifest primarily as reversible hydrostatic pressure changes rather than interfacial shear loading. To manage this, we codesign the RDL thickness to enhance bending stiffness,

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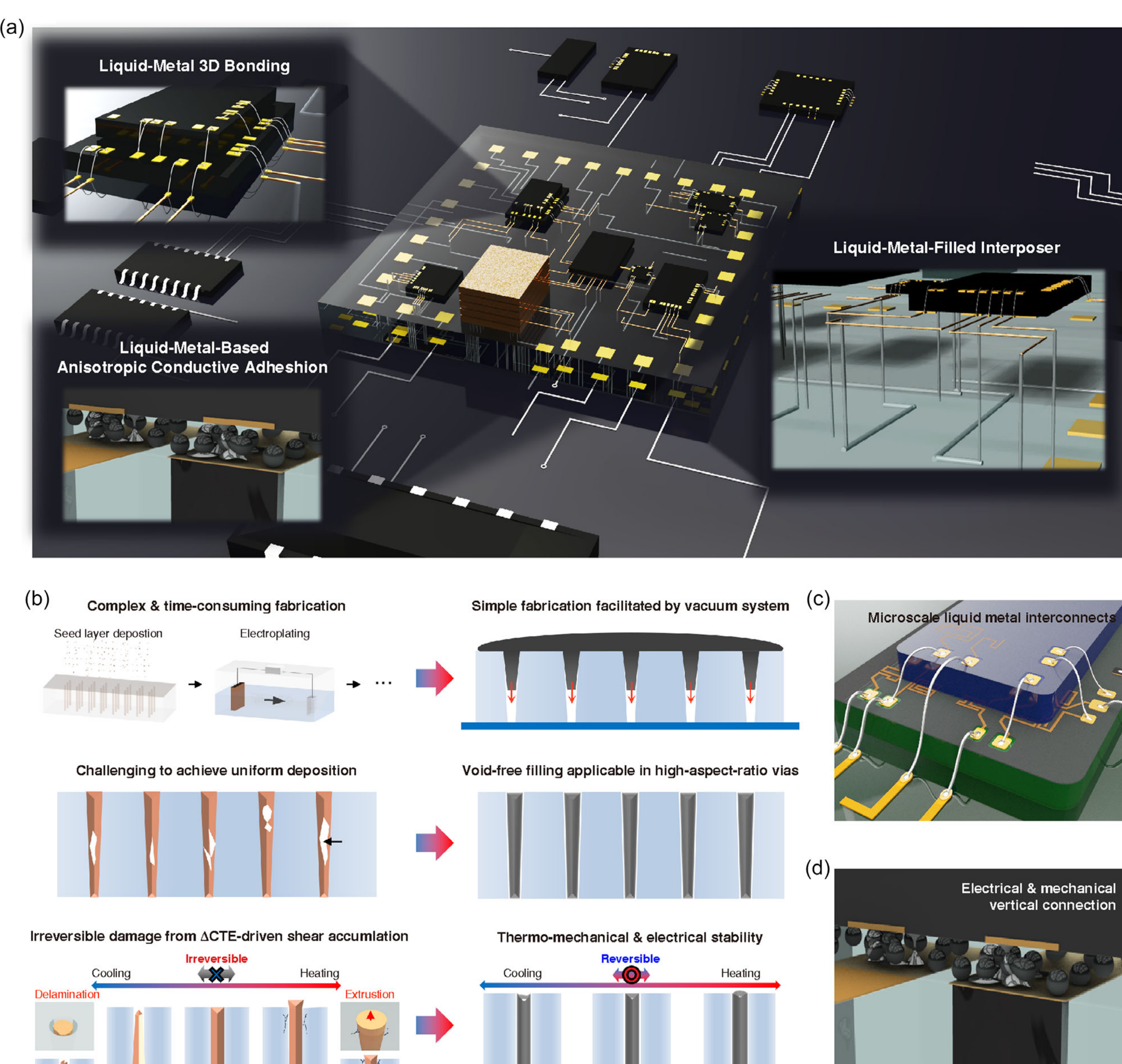

FIGURE 1 | A universal LM interconnect platform for 2.5D glass packaging. (a) Schematic overview of the proposed platform, comprising LM-filled TGVs, 3D direct-printed LM interconnects, and LM-ACA for interfacial bonding. (b) Comparison between conventional copper-filled TGVs (left) and LM-filled TGVs (right). The LM approach eliminates the need for seed layer deposition and electroplating, enabling void-free filling in high-aspect-ratio structures. Moreover, the hydrostatic nature of LM supports a shear-free load path, while a stiffness-optimized RDL confines deformation to a reversible elastic regime, enhancing both thermomechanical and electrical stability. (c) Schematic of 3D LM interconnects enabling fine-pitch routing. (d) LM-ACA enabling reliable vertical electrical and mechanical connections from chip to interposer to PCB, under low thermal and pressure conditions. LM = Liquid metal; LM-ACA = liquid metal-based anisotropic conductive adhesive; RDL = redistribution layer; TGVs = through-glass vias.

which confines deformation to a small, elastic regime and prevents cap bowing. This shear-free, pressure-dominated loading condition, combined with optimized RDL design, ensures robust thermomechanical and electrical reliability without geometric distortion. Figure 1c illustrates 3D microprinted LM interconnects bridging chip pads to either adjacent chips or the interposer. The direct-printing process achieves line widths on the order of 5 µm, surpassing the ≈20 µm pitch limitation of conventional wire bonding and enabling high-density routing. A six-axis motion system offers micrometer-scale control in x, y, and z directions, along with fine angular precision, supporting complex and fully 3D routing. Figure 1d illustrates LM-ACA that provides vertical electrical pathways and mechanical adhesion without requiring solder reflow or thermocompression. By eliminating high temperature and pressure, this method supports panel-scale assembly while ensuring stable, low-resistance contact.

2.2 | Vacuum-Assisted Capillary Infiltration of Liquid Metal into Through-Glass Vias

Figure 2a presents a schematic of the LM-filled interposer, in which TGVs are filled with LM and top and bottom RDLs are formed by metallization and patterning. TGVs with a radius of

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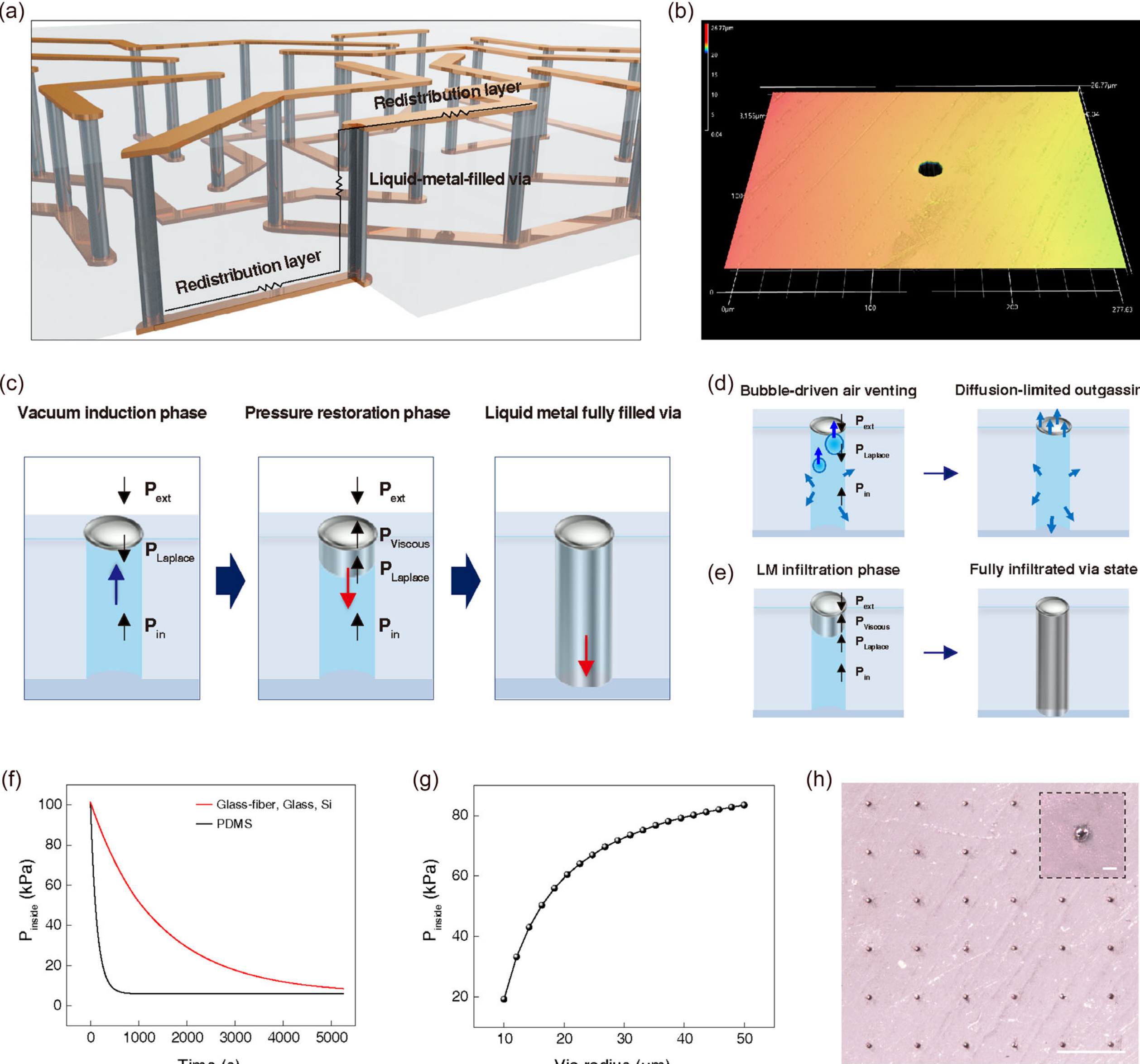

FIGURE 2 | **LM filling of TGVs.** (a) Schematic illustration of a LM-filled interposer (LM-interposer). (b) 3D LSCM image of a via hole in a glass-fiber-reinforced substrate. (c) Schematic of the LM filling process via VACI: vacuum induction phase (left), pressure restoration phase (center), and final filled state (right). (d) Air evacuation mechanisms during the vacuum induction phase: bubble-driven venting (left) and diffusion-limited outgassing (right). (e) LM infiltration process during the pressure restoration phase, leading to complete via filling. (f) Variation in internal via pressure during the vacuum induction phase for different substrate materials (glass-fiber, glass, silicon, and PDMS). (g) Maximum pressure required for full LM infiltration as a function of via diameter. (h) OM image showing a via array uniformly filled with liquid metal. Scale bar, 200 μm, and inset: scale bar, 20 μm. LM = Liquid metal; LSCM = laser scanning confocal microscope; OM = optical microscope; VACI = vacuum-assisted capillary infiltration.

10 μm were laser-drilled into a 150 μm-thick glass-fiber substrate using a femtosecond laser. A 3D laser-scanning confocal micrograph confirms a clean, well-defined via profile (Figure 2b). The vias were then filled with LM using simple VACI at room temperature. To enable VACI filling, a polydimethylsiloxane (PDMS) sealing layer (thickness, 5 mm) was applied to seal the via bottoms, creating a single-entry geometry for controlled infiltration. An EGaIn layer was then applied to cover the via openings, and the assembled sample was loaded into a vacuum chamber. Pressure cycling, in which the chamber pressure is first lowered and then restored to ambient, evacuates trapped air from the vias and replaces it with LM, thereby producing LM-filled TGVs. EGaIn can fill complex microstructures conformally without plating, curing, or high-temperature steps based on low viscosity (≈2.4 mPa·s) [20, 21]. As a result, an EGaIn-filled via naturally forms an ultrasmooth surface without the rough crystalline sidewalls or seams typical of electroplated Cu vias.

To analyze the mechanism by which TGVs are filled with LM, the process is divided into two phases (Figure 2c). In the vacuum induction phase, lowering the chamber pressure (P_{ext}) promotes air evacuation from the vias. In the pressure restoration phase, returning P_{ext} to ambient drives LM infiltration via capillary action and the induced pressure differential, thereby completing the fill. We further divide the vacuum induction phase into two

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stages based on the dominant pathway for air evacuation. Bubble-driven air venting dominates early, whereas diffusion-limited outgassing of residual trapped air predominates later (Figure 2d). In the early bubble-driven air venting regime, the pressure differential across the LM–air meniscus exceeds the Laplace pressure barrier, allowing large bubbles to nucleate, coalesce, and displace the overlying EGaIn, thereby enabling air escape. This is followed by a diffusion-limited outgassing regime, in which residual trapped air is gradually removed by diffusion through the PDMS bottom sealing layer and the LM droplet at the TGV inlet.

To better understand the VACI process, we developed a physical model and carried out an analytical analysis. Through this model, we elucidate the mechanism of air evacuation from the TGV and determine the conditions required for complete LM filling. Specifically, we employ the Young–Laplace relation to capture curvature-dependent capillary pressures at the LM–air interface, the Hagen–Poiseuille equation to describe viscous flow in cylindrical conduits, and Fick's law to model diffusive gas transport. Together, these relations enable a systematic analysis of how pressure differentials, interfacial tension, viscous flow, and diffusion kinetics contribute to air evacuation from TGVs and LM ingress. The time-dependent pressure change $P_{\mathrm{inside}}(\mathrm{t})$ inside the TGV during the vacuum induction phase is given by Equation (1), with the detailed derivation and explanation provided in Supplementary Note 1.

$$P_{\mathrm{inside}}(\mathrm{t}) = \begin{cases} P_{\mathrm{ext}} + (P_0 - P_{\mathrm{ext}})\mathrm{e}^{-\frac{\mathrm{t}}{\tau_{\mathrm{bubble+diffusion}}}}, & \text{(Bubble-driven release)} \\ P_{\mathrm{ext}} + (P_{\mathrm{transition}} - P_{\mathrm{ext}})\mathrm{e}^{-\frac{(\mathrm{t} - \mathrm{t}_{\mathrm{bubble+diffusion}})}{\tau_{\mathrm{diffusion,total}}}}, & \text{(Diffusion-driven decay)} \end{cases} \quad (1)$$

where the relevant parameters are defined as follows. $P_{Laplace}$ is the Laplace pressure at the LM–air meniscus; $\tau_{bubble+diffusion}$ is time constant for combined bubble-driven and wall-diffusion air release; $\tau_{diffusion,total}$ is time constant for full diffusion-limited regime; $P_{transition}$ is the internal pressure at the regime transition; and $t_{bubble+diffusion}$ is time at which the bubble-to-diffusion transition occurs.

After the vacuum induction phase, once the trapped air has been evacuated, the high surface tension of the LM temporarily blocks the via inlet. As the chamber pressure is returned to ambient, the process enters the pressure restoration phase (Figure 2e). The LM at the via inlet is driven inward, leading to full infiltration of the via. To formalize the restoration phase, we derive boundary conditions in Equations (2) – (4) that link the capillary entry pressure, the recovery of external pressure, and the motion of the LM meniscus.

$$P_{\mathrm{ext-af}}\{t_{\mathrm{start}}\} - P_{\mathrm{in},s} = P_{\mathrm{Laplace}} \quad (2)$$

$$P_{in}(t) = \frac{P_{in,s} \cdot L}{L - x(t)} \quad (3)$$

$$L = \int_{t_{start}}^{t_{fullfill}} v(t)dt \quad (4)$$

Using these boundary conditions, we model the LM ingress dynamics with Python-based numerical simulations, computing critical thresholds and trajectories. The model yields the maximum $P_{\mathrm{in,s}}$ that ensures complete infiltration during pressure restoration phase. From this sequence, we determine the initial internal pressure in the via required for complete infiltration. The computed internal pressure is correlated with the end-of-induction vacuum pressure about Equation (1), which in turn define the required chamber vacuum pressure conditions in the preceding vacuum induction phase.

The entire VACI process was analyzed through computational simulations, and the experimental conditions were derived by incorporating our chamber vacuum environment and via parameters. During the vacuum induction phase, the internal pressure variation within the vias differed depending on the material of the via substrate (Figure 2f). PDMS substrates exhibit rapid pressure decay due to their high gas permeability, whereas glass, glass-fiber, and Si substrates show slower decay [22]. Figure 2g presents the maximum internal pressure required for complete filling as a function of TGV diameter. Because the substrate thickness was fixed at 150 µm, the diameter-dependent filling behavior corresponds to variation in via aspect ratio (height/diameter). For our fabricated 20 µm-diameter TGVs, the internal via pressure needed to be reduced to 58.5 kPa to achieve complete LM filling. Under our experimental chamber conditions, this was achieved by maintaining vacuum for 35 min before releasing the pressure to initiate LM infiltration. In the present VACI process, the PDMS layer serves only as a temporary sealing aid to seal the via bottom, establish a single-inlet geometry, and maintain the pressure conditions required for complete LM infiltration, and is removed after filling (Figure S1). We further evaluated the effect of PDMS sealing-layer thickness on LM filling (Figure S2). We successfully filled 6 × 6 arrays of 20 µm-diameter TGVs with LM, and optical microscopy confirmed uniform infiltration across the array (Figure 2h). In addition, SEM images of LM-filled TGVs with different via aspect ratios further support the applicability of the VACI process across a range of TGV geometries (Figure S3).

2.3 | Structural and Electrical Characterization of the Liquid Metal-Filled Interposer

To fabricate the LM-interposer, we filled TGVs (10 µm in radius, 150 µm in height) with LM, followed by top and bottom metal deposition to form RDLs (Figure 3a). A Cu seed layer was deposited to enable uniform Cu electroplating, after which the Cu layer was electroplated and patterned photolithographically to define the interposer RDLs. Prior studies have shown that the Cu–EGaIn interface remains remarkably stable over long-term contact, forming only a thin Cu–Ga intermetallic layer that significantly slows Ga diffusion and maintains stable contact resistance even after 1000 h of aging at temperatures up to 100°C [23]. To verify complete LM filling in the TGVs, the LM-interposer was milled using focused ion beam (FIB), and the cross section was imaged by scanning electron microscopy (SEM) (Figure S4). Figure 3b shows a colorized SEM image (blue for LM, green for the interposer substrate, and orange for Cu). The vias are completely filled with LM, showing no detectable voids, and the LM–glass interface is continuous, gap-free, and stable. Elemental mapping by energy-dispersive spectroscopy (EDS) identifies the spatial distributions of Si and Ga, corroborating the structural assignment.

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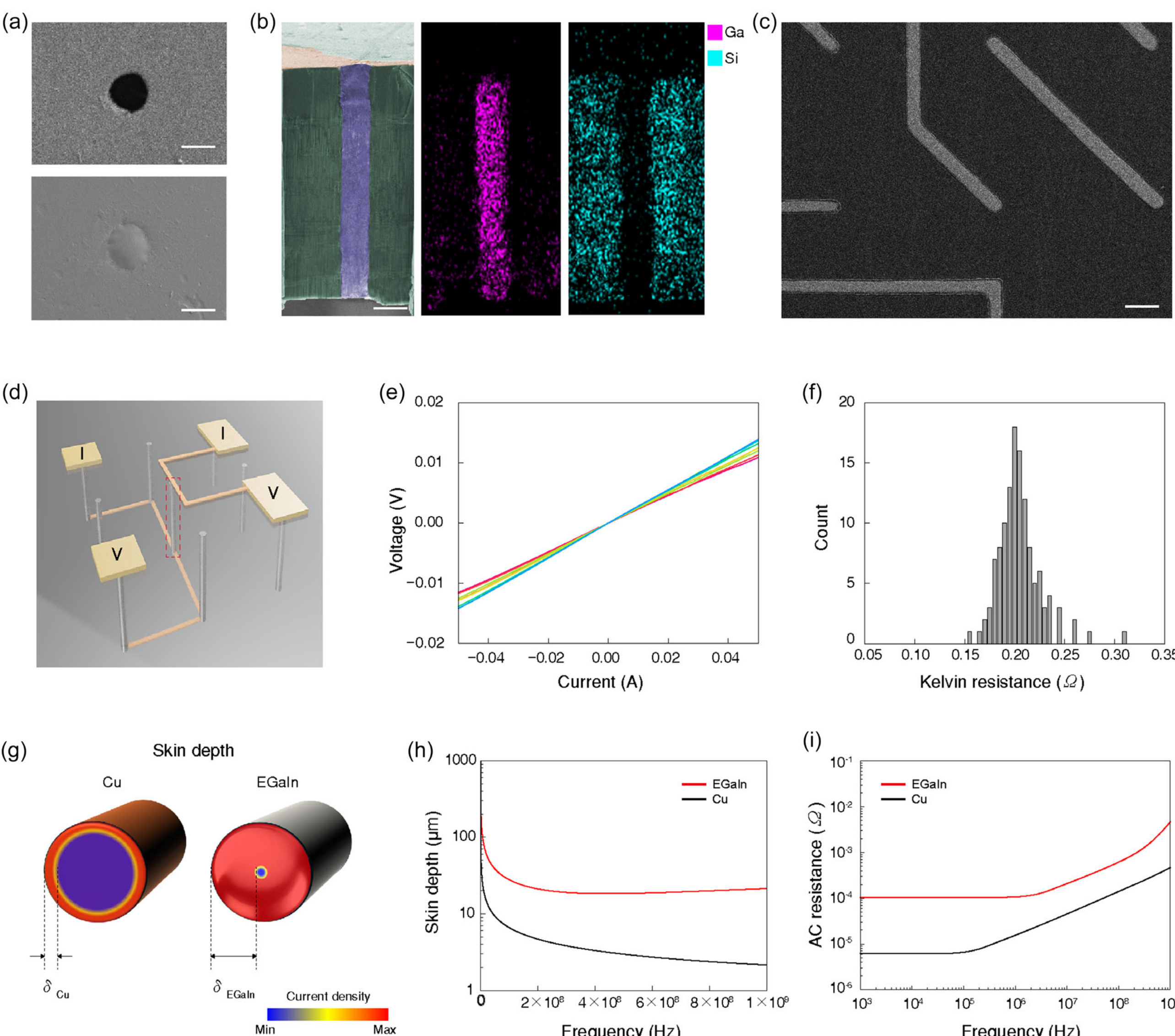

FIGURE 3 | **Electrical properties of LM-filled glass interposers.** (a) SEM images of glass vias before (top) and after (bottom) filling with LM. Scale bars, 20 μm. (b) Colorized SEM image of a FIB cross section of an LM-filled TGV (left), with corresponding EDS elemental maps showing Si (middle) and Ga (right). Scale bar, 20 μm. (c) SEM image of an LM-filled interposer after Cu electroplating and patterning. Scale bar, 50 μm. (d) Schematic of a Kelvin test structure used to measure the four-point resistance of LM-filled TGVs. (e) Representative current–voltage (*I*–*V*) curves measured from 10 individual LM-filled TGVs. (f) Statistical distribution of four-point Kelvin resistances. (g) Schematic illustration comparing current density distributions in copper (Cu) and eutectic gallium–indium (EGaIn) due to differences in skin depth under AC excitation. (h) Frequency-dependent skin depth of Cu and EGaIn. (i) AC resistance of Cu- and LM-filled TGVs, calculated from material conductivity and skin depth. EDS = Energy-dispersive spectroscopy; LM = liquid metal; SEM = scanning electron microscope; TGV = through-glass via.

To ensure structural and electrical stability under temperature excursions, we implement an interface stabilization strategy by designing a stiffness-optimized RDL that supports the hydrostatic load imposed by LM-filled TGVs while preserving geometric integrity. Although EGaIn is liquid at room temperature and does not sustain static shear, its thermal expansion induces a normal hydrostatic pressure on the confining cap layer [24]. If the cap is insufficiently stiff, this load can lead to elastic bulging or, in thin/fragile stacks, to delamination or leakage. We therefore increased the RDL thickness to enhance bending stiffness, minimizing elastic deflection and ensuring that operating stresses remain below thresholds for irreversible damage. To determine the RDL thickness required to withstand temperature-induced deformation in LM-filled TGVs, we modeled the LM-TGV system as a sealed, void-free via embedded within a rigid substrate, as detailed in Supplementary Note 2. Under a temperature variation of $\Delta T = 160$ K (−40 to 120°C), the internal pressure induced by the thermal expansion of LM increases by approximately $\Delta p \approx 0.35$–0.46 GPa. We model the metal cap as a clamped circular thin plate subjected to a uniform pressure Δp. To ensure mechanical integrity, we compute the required RDL thickness t by applying small-deflection plate theory to determine the peak stress (Equation 5) .

$$\sigma_{\max} \approx C(\nu)\frac{pa^2}{t^2},\ C(\nu) = \frac{3+\nu}{8} \tag{5}$$

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where $\nu_{Cu} \approx 0.34$ is the Poisson's ratio of Cu, $C \approx 0.4175$ is a constant from plate theory, and t is the effective metal thickness. Based on the target stress range of electroplated Cu (200–500 MPa), the required metal thickness was calculated to be between 5.66 and 8.95 µm [25, 26]. Accordingly, we electroplated a ≈10 µm-thick Cu layer under controlled conditions (0.005 Vs^{-1} for 10 min), followed by photolithographic patterning to define the RDL structure (Figure 3c). The LM-interposer demonstrated structural and electrical stability following thermal cycling between −40°C and 120°C (Figures S5 and S6). To further assess long-term reliability under combined heat and humidity stress, we performed 85°C/85% RH damp-heat aging tests and monitored both the mass change and resistance change of the LM interconnect platform. Negligible mass variation and stable electrical resistance were observed throughout the test period, indicating no evident leakage and sustained electrical stability under accelerated aging conditions (Figures S7 and S8).

To evaluate the electrical performance of the LM-interposer, we fabricated a Kelvin structure and measured DC resistance using a four-point probe method (Figure 3d) [27]. Figure 3e shows a representative I–V curves of a single TGV (20 µm in diameter, 150 µm in length), which exhibit a resistance of ≈200 mΩ. The resistance distribution measured across 78 TGVs is plotted as a Gaussian histogram (Figure 3f), indicating consistent and uniform resistance across the interposer array. Since glass interposers are intended to operate under high-frequency conditions, understanding the behavior of AC resistance in the MHz–GHz range is particularly critical. A potential concern lies in whether the LM can adequately compensate for the electrical conductivity of Cu, which is typically used in conventional TGVs. At frequencies above several MHz, Cu experiences substantial skin effect, where the current is confined to a very thin surface layer (Figure 3g) [28, 29]. However, the skin effect has been reported to be reduced in EGaIn compared to Cu in previous studies, which indicates that LM can sustain a substantial current-carrying capacity by distributing current over a larger cross-sectional area at high frequencies [17]. To verify this, we calculated the skin depths as a function of frequency using the standard skin depth equation, based on the conductivity values of electroplated Cu and EGaIn (Equation (6)) (Figure S9, SI). The calculated results show that the skin depth of Cu is ≈7 µm at 1 MHz and narrows to about 2 µm at 1 GHz, whereas that of EGaIn remains much larger, at around 50 and 40 µm at the same frequencies, respectively (Figure 3h).

$$\delta\{\omega\} = \sqrt{\frac{2}{\omega\mu\sigma}}\{\omega = 2\pi \mathrm{f},\ \mu \approx \mu_0 = 4\pi \times 10^{-7}\mathrm{H/m}\} \quad (6)$$

where $\omega = 2\pi f$, $\mu \approx \mu_0 = 4\pi \times 10^{-7} H/m$, and σ is the electrical conductivity.

$$Z\{\omega\} = Z'\{\omega\}\, L,\ Z'(\omega) = \frac{k}{\sigma\, 2\pi a}\frac{J_{0(k(w)\cdot a)}}{J_{1(k(w)\cdot a)}} \quad (7)$$

where $k(\omega) = \sqrt{i\omega\mu\sigma}$ is the complex propagation constant, J_0 and $J_1$are Bessel functions of the first kind (orders 0 and 1), and a is the via radius.

To evaluate the frequency-dependent AC resistance considering the skin effect, we use scattering parameters reported in previous studies [30, 31]. From these data, we extract the frequency-dependent complex permittivity (or equivalently, the effective conductivity) of the EGaIn via material by fitting to the Drude free-electron model and using full-wave electromagnetic simulations (CST Studio) for validation. We applied Maxwell's equations in cylindrical coordinates and solved the Bessel function formulation (Equation (7)) for a uniformly filled single TGV for both Cu-filled and EGaIn-filled vias (Figure 3i). This approach allows us to directly compare the high-frequency electromagnetic performance of EGaIn against that of Cu and other conductors. We find that the EGaIn-filled vias exhibit consistently lower insertion loss per length at high frequencies than Cu-filled vias of similar geometry, particularly at the upper end of the MHz spectrum. The extracted complex permittivity of EGaIn shows a relatively flat real part (metallic behavior) and a modest imaginary part (loss factor) that increases with frequency, in line with Drude-model predictions for a metal with finite carrier relaxation time [32]. Notably, when benchmarking EGaIn against Cu, the effective loss tangent of the EGaIn via is smaller than that of a Cu via above a certain frequency (≈5–10 MHz), despite EGaIn being less conductive at DC. We attribute this phenomenon to the dominance of surface scattering and skin-depth limitations in the Cu vias. As frequency rises, the Cu's effective cross-sectional area for current becomes extremely small (skin effect) and the rough Cu surface causes additional Ohmic loss, whereas the EGaIn via, with its smooth interface, retains a larger effective conduction area and incurs lower incremental loss. This is consistent with the understanding that conductor surface roughness and high-frequency current crowding are major causes of RF loss in interconnects [33, 34]. This result indicates that the lower conductivity of EGaIn can be effectively compensated for by its reduced skin effect.

2.4 | Liquid Metal 3D-Printed Interconnects for Heterogeneous Packaging

We present free-standing LM interconnections that bridge chip-to-chip and chip-to-interposer RDL pads using a pneumatic, six-axis microprinting system (Figure 4a). The platform comprises a pressure-controlled LM reservoir and a glass micronozzles mounted on a six-axis motion stage, which together enable precise control of both the reservoir pressure and nozzle motion to define the shape and trajectory of the LM interconnection [35]. Figure 4b outlines the lift-off sequence for spanning pads at different heights. The process begins by printing LM from the first pad toward the opposite pad (i). A short backward printing step forms an initial 3D interconnect backbone (ii), followed by gradual nozzle lifting to create a freestanding arch (iii). Finally, the nozzle is lowered to contact the second pad, completing the 3D LM interconnect (iv). The intrinsic oxide layer (≈1 nm) that forms on the LM surface provides mechanical integrity, enabling the printed LM interconnections to retain their 3D geometry [36, 37]. Using this system, we connected all 24 pads surrounding a 200 µm-tall chip via LM 3D printing on all four sides (Figure 4c). The LM line width is tunable by adjusting the nozzle's inner diameter and the stage speed. Figure 4d presents the measured line widths at a fixed printing speed of 1 mm s^{-1} for different nozzle sizes. Successful lift-off requires the z-stage to descend within a bounded speed window (Figure 4e). If the z-axis

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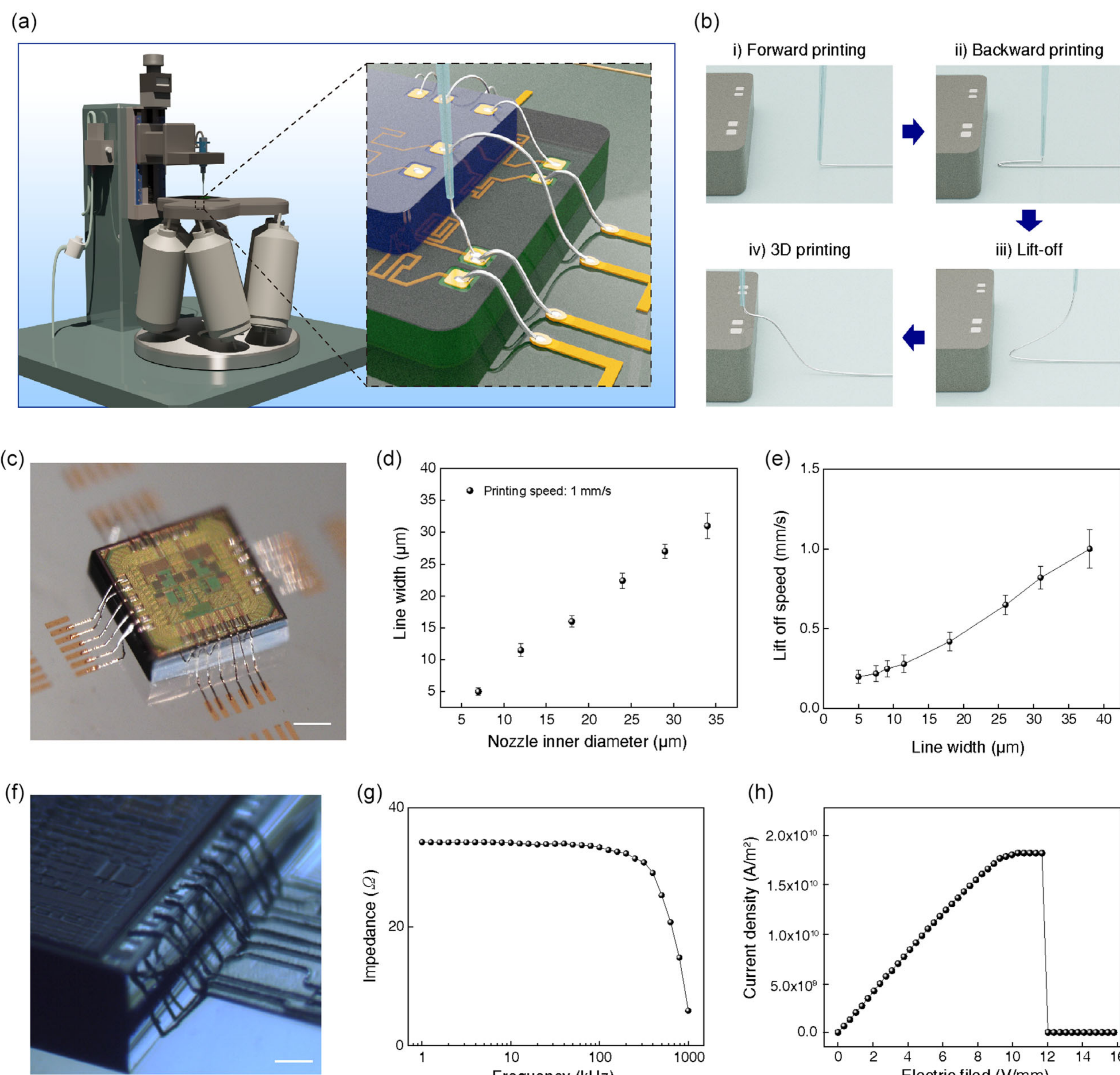

FIGURE 4 | **LM 3D-printed interconnects for heterogeneous packaging.** (a) Schematic of the LM 3D printing system with pneumatic control and six-axis stage, forming freestanding metal traces that bridge chip-to-chip and chip-to-interposer RDL pads. (b) Process of 3D LM printing between pads with vertical offset. (c) OM image of a packaged chip connected to surrounding pads via four-sided freestanding LM interconnects. Scale bar, 300 μm. (d) Printed LM line width as a function of the inner diameter of the glass nozzle (at constant printing speed of 1 mm s^{-1}). (e) Required *z*-axis lift-off speed for stable LM line detachment. (f) Microscope image of a 3D LM interconnect bridging a chip pad and an interposer RDL pad with vertical height difference. Scale bar, 200 μm. (g) Frequency-dependent impedance of a single 3D LM interconnect. (h) Current density response of the LM interconnect under AC bias. LM = Liquid metal; OM = optical microscope; RDL = redistribution layer.

descent is too fast, the 3D interconnect necks and breaks because mechanical integrity of oxide layer cannot be maintained. If it is too slow, surface tension exceeds LM-substrate adhesion, causing the LM to grow vertically into a pillar until the nozzle reservoir is locally depleted. We demonstrate nine parallel LM 3D interconnects bridging a chip-pad array and RDL pads patterned on a glass interposer (Figure 4f). The impedance characteristics of a single LM filament are shown in Figure 4g, exhibiting a decrease in impedance with increasing frequency. Under an AC bias, we measured the resistance of the 3D-printed EGaIn interconnect. The current density increased nearly linearly with the electric field and reached 1.89×10^{10} A m^{-2} just before breakdown (Figure 4h). This value is comparable to that of vacuum-deposited Au, Al, and Cu films ($\approx 10^{10}$ A m^{-2}), indicating that the printed EGaIn interconnect can carry high current under AC operation [36]. To further evaluate the thermal characteristics of the 3D-printed LM interconnect under high-power operation, we performed infrared (IR) thermography during electrical loading. The IR images reveal the spatial temperature distribution of the freestanding LM interconnect, and the maximum temperature rise increased with input power (Figures S10 and S11). Additional mechanical reliability tests under cyclic bending and

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vibration fatigue loading further demonstrated the structural and electrical stability of the 3D-printed LM interconnect (Figures S12 and S13).

2.5 | Development and Characterization of Liquid Metal-based Anisotropic Conductive Adhesive

We developed an LM-ACA to make electrically and mechanically interconnect the LM-interposer and electrode pads at room temperature (Figure 5a). To enable fine-pitch bonding, LM was dispersed in solvent via bar sonication, yielding uniformly sized LM microcapsules. Taking advantage of the LM's native oxide skin, we produced core–shell structures in which the LM is confined beneath a thin, conformal oxide skin. Capsule diameter was tuned by adjusting sonication power and duration, achieving $1.97 \pm 0.68 \mu m$ (Figure 5b). Under applied pressure, the oxide shells rupture and the LM percolated, forming vertical conductive paths so that bonding proceeds entirely at room temperature without the need for thermal curing. We validated the electrical conduction of LM-ACA, and Figure 5c plots the through-thickness and in-plane conductivities versus LM-capsule loading, showing that for 40–70 wt% LM, the film exhibits high anisotropy with vertical resistance about 5 Ω and lateral resistance greater than 118 MΩ. To evaluate bonding performance with actual devices, we used LM-ACA to connect eight chip pads to patterned gold electrodes (A1–A8), where only A1 and A8 were originally electrically connected (Figure 5d). After bonding, resistance measurements between A1 and the other pads (A2–A8) showed that only the A1–A8 pair exhibited a significantly lower resistance, confirming that the LM-ACA established selective and reliable electrical connections while maintaining insulation between unbonded pads (Figure 5e).

We further investigated the force-dependent electrical response and contact resolution of LM-ACA. Using a force gauge (Mark-10, USA), a normal force was applied while monitoring resistance across LM-ACA samples of varying thickness (Figure S14). For LM-ACA thicknesses of 5, 7, and 10 µm, the contact onset forces were about 5, 21, and 45 N, respectively (Figure 5f). Resolution tests as a function of electrode line width and spacing showed vertical resistances of ≈5 Ω and no measurable lateral leakage down to 10 µm spacing (Figure 5g). Mechanical adhesion was assessed via a 180° peel test, in where LM-ACA was spin coated onto a PET film and peeled in the vertical direction to measure the maximum peel force (Figures 5h and S15, SI). C5 resin (quintone) was added in varying amounts (0.21 g, 0.32 g, 0.42 g) to optimize adhesive strength. The maximum peel strength of 5.1 N was achieved with 0.42 g of C5 resin. We further evaluated the stretchability of the LM-ACA by applying tensile strain and measuring the corresponding tensile stress (Figure S16). Additionally, shear strain tests confirmed negligible changes in electrical resistance even under shear strains exceeding 100% (Figure S17). Collectively, the LM-ACA supports large-area, panel-level integration, as demonstrated by uniform coatings on substrates larger than 7 × 7 cm, indicating compatibility with scalable interposer and PCB-level applications (Figure S18). It is also suitable for high-resolution circuits and heterogeneous device integration, enabling precise, low-temperature bonding.

2.6 | System-Level Demonstration of Integrated Liquid Metal-Based Packaging Technologies

To demonstrate the applicability of LM-based heterogeneous packaging at the system level, we integrated three key technologies, LM-filled TGVs, 3D-printed LM interconnects, and

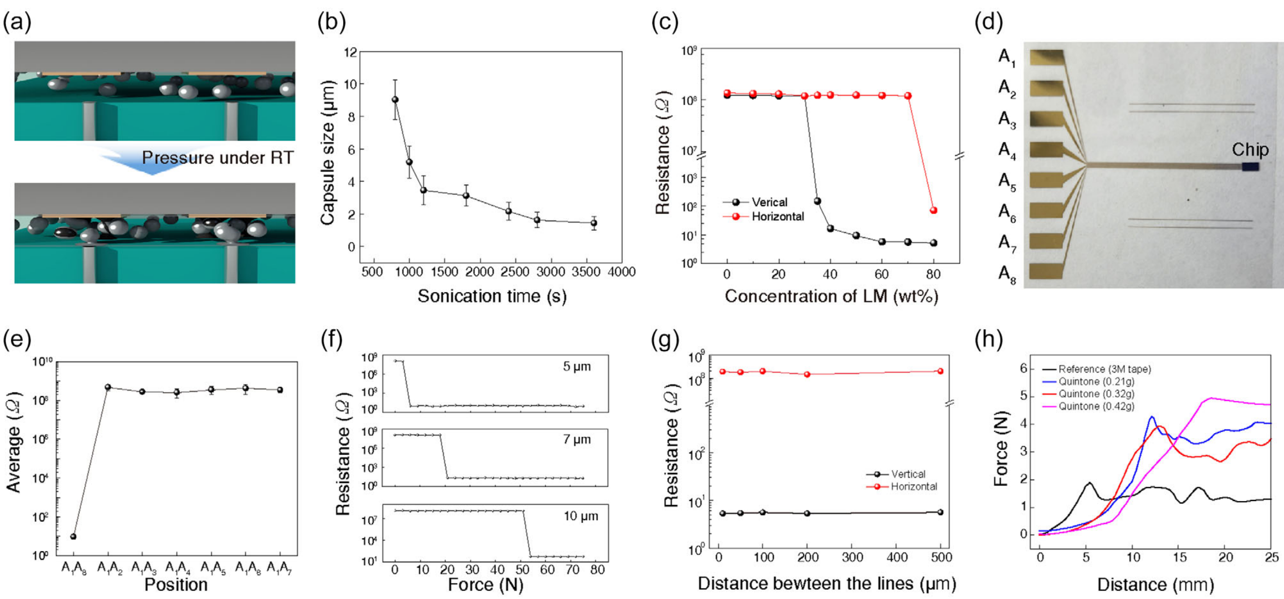

FIGURE 5 | | LM-ACA. (a) Schematic illustration of LM-ACA under room-temperature pressure bonding. (b) Average capsule diameter as a function of sonication time. (c) Electrical resistance of the LM-ACA in vertical and horizontal directions as a function of LM capsule concentration. (d) Photograph of a chip bonded to gold interconnect electrodes using LM-ACA. (e) Measured resistance at each electrode pair shown in (d). (f) Resistance of LM-ACA under varying bonding force for various thicknesses (5, 7, and 10 µm). (g) Electrical anisotropy of LM-ACA shown as resistance versus electrode spacing. (h) Adhesion force profile of LM-ACA compared with commercial adhesive tapes. LM-ACA = Liquid metal-based anisotropic conductive adhesive.

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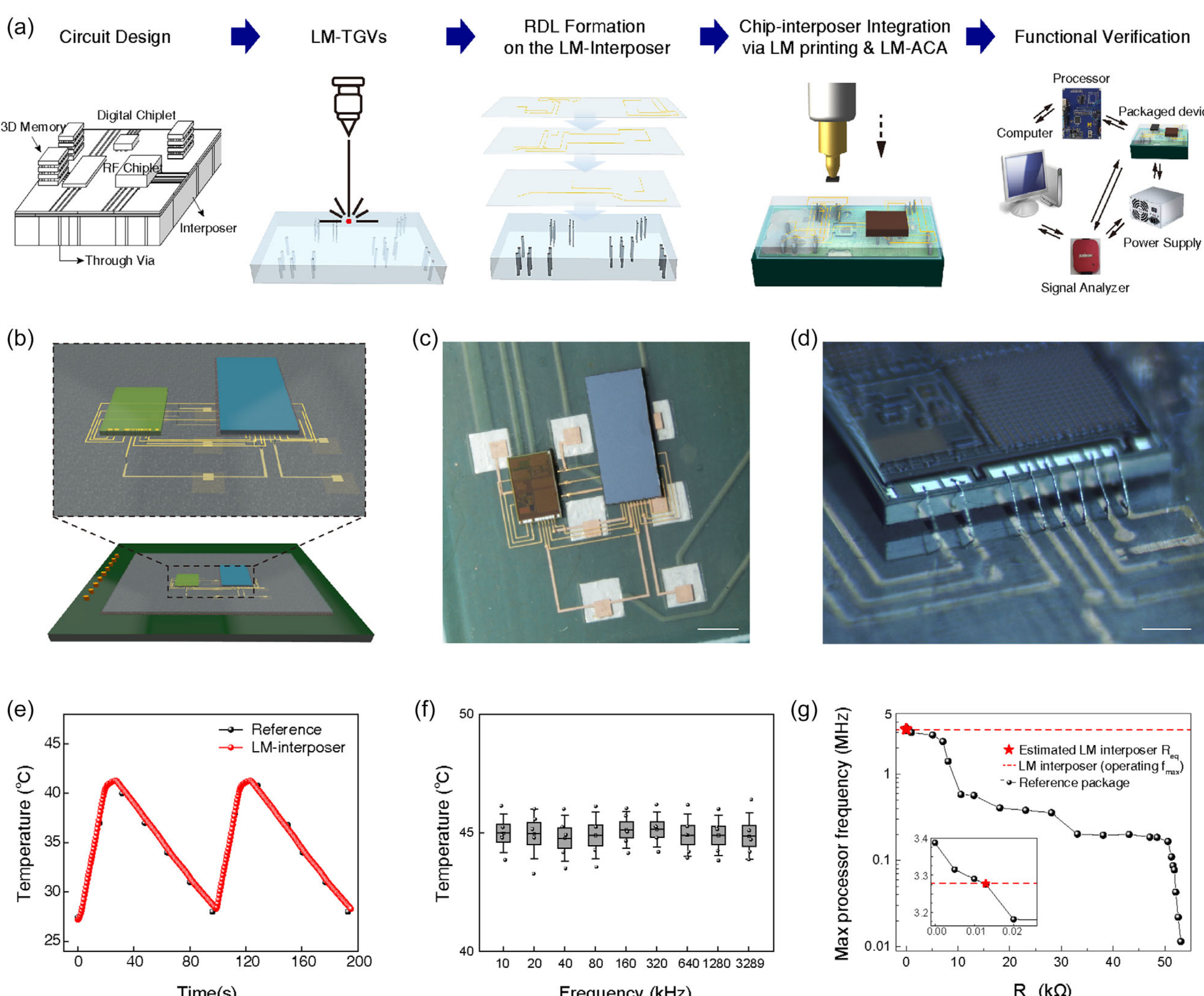

FIGURE 6 | | System-level demonstration of the LM-interposer platform. (a) Workflow schematic for fabricating a LM-filled interposer. (b) Schematic of an integrated package using the LM-interposer, featuring LM-filled TGVs and RDLs. (c) Photograph of an assembled LM-interposer system for demonstration consisting of two chips mounted on an LM-interposer and connected to a PCB. Scale bar, 1 mm. (d) 3D OM image showing 3D-printed LM interconnects bridging chip pads and interposer RDLs. Scale bar, 200 µm. (e) Real-time temperature measurements of the LM-interposer-based sensor during cyclic operation. (f) Temperature readouts across various operating frequencies, showing stable sensing performance around 45°C. (g) Estimation of the equivalent series resistance (R_{eq}) of the LM-interposer. A reference package with inserted series resistors was used to calibrate the relationship between maximum operating frequency (f_{max}) and R_{eq}. Projecting the LM-interposer's f_{max} (3,279 kHz; horizontal red-dashed line) onto the reference curve yields $R_{eq} \approx 13\ \Omega$. The inset shows a magnified view of the frequency range from 3,130 kHz to 3,400 kHz. LM = Liquid metal; OM = optical microscope; RDL = redistribution layer; TGVs = through-glass vias.

LM-ACA bonding, into a high-density electronic system. Figure 6a illustrates the overall fabrication workflow for LM-packaging. The process begins with circuit design and the formation of TGVs at designated locations in the glass-fiber substrate by femtosecond-laser drilling (Figure S19 and 20). The TGVs are then filled with LM via VACI, after which top- and bottom-side RDLs are defined. Two chips are mounted and electrically connected to the top-side RDLs using either 3D-printed LM interconnects or LM-ACA. Then, the chip integrated LM-interposer is integrated with a PCB by applying LM-ACA to the bottom-side RDLs.

The complete package consists of two chips placed side-by-side atop the interposer (Figures 6b, S1 and S21), each connected to the top-side RDLs via either LM 3D bonding or LM-ACA. The interposer incorporates nine LM-filled TGVs that provide vertical signal paths between the top-side chips and the bottom-side RDLs. The LM-filled interposer integrated with the chips was connected to the PCB via LM-ACA bonding (Figure 6c). Figure 6d shows a chip with eight pads successfully connected to the interposer's RDLs using 3D LM bonding. The fully assembled system, referred to as the LM-package, was interfaced with an system programming board, power supply modules, and signal analyzers to demonstrate functionality. The signal and power line routing for this system-level integration is shown in Figure S22. To evaluate operational stability and compatibility with sensor integration, real-time temperature monitoring was implemented using the LM-package (Figure S23). Figure 6e shows that the system accurately measured temperature, with close agreement between the IR camera measurements and the sensor output. Moreover, the LM-packaging

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system maintained consistent performance across a broad frequency range from 10 kHz to 3.279 MHz, successfully detecting temperatures near 45°C (Figure 6f). We further compared the LM-interposer package with a conventional PCB-based package, which served as a reference for performance evaluation. In reference packages, as shown in Figure 6g, additional series resistance in the interconnects reduces the maximum operating frequency of the processor. To quantitatively compare performance, equivalent resistance (R_{eq}) was incrementally added to a reference package, and the corresponding maximum operational frequency was measured. By projecting the LM-interposer's maximum operating frequency (3.279 MHz; horizontal red line) onto the reference package curve, we estimate an added equivalent series resistance of ≈13 Ω. This suggests that the LM-interposer package performs comparably to a commercial system with 13 Ω of added interconnect resistance. Thus, relative to the conventional package, the LM-interposer introduces only a small additional series resistance while enabling low-temperature assembly, fine-pitch 3D routing, and panel-scale compatibility.

3 | Conclusions

In summary, we have established an LM-based interconnect platform that integrates LM into the complete 2.5D glass interposer process, offering a unified and scalable solution for advanced heterogeneous packaging. Using VACI, we achieved conformal and void-free metallization of high-aspect-ratio TGVs without the need for seed-layer deposition or electroplating, thereby lowering the thermal budget and reducing both cost and process complexity. A stiffness-optimized RDL structure was codesigned to accommodate the hydrostatic pressure from the LM, effectively suppressing shear accumulation and preserving structural and electrical integrity under thermal stress. Furthermore, 3D microprinting of LM enables freestanding interconnects with sub-5 µm linewidths, facilitating direct chip-to-chip and chip-to-interposer bridging. An LM-ACA provides vertical electrical conduction and mechanical adhesion entirely at room temperature and low pressure, enabling reliable panel-scale integration. This approach accommodates height variations between chips and interposers and supports bonding to nonplanar or rough surfaces, thereby increasing the flexibility of heterogeneous system assembly. By integrating these three technologies, we demonstrated a functional LM-filled interposer system that reliably performed real-time temperature monitoring and chip-to-chip communication across 10 kHz to 3.279 MHz [38, 39]. The LM-interposer introduced only minimal additional resistance and achieved electrical performance comparable to that of conventional packages. LM consistently maintained electrical performance comparable to Cu, with negligible skin-effect losses at high frequencies, while also delivering enhanced thermomechanical compliance.

Although the long-term reliability of LM-based systems requires further study, including sealing strategies, leakage control, electrochemical stability, and material compatibility under operational stress, the intrinsic stress-relieving properties and potential for self-healing make LM a particularly promising material for robust and scalable system integration. Looking ahead, improvements in panel-scale process control and validation of LM compatibility with diverse chiplet types, including power management, wireless communication, and memory dies, will be critical to enabling large-scale industrial adoption. This study represents a significant step forward in the integration of materials, processes, and system architectures for high-density and high-frequency glass interposer platforms. Our findings collectively position LM as a manufacturable and reliable interconnect medium that addresses key bottlenecks in performance, integration, and scalability for future heterogeneous electronics.

4 | Experimental Section

4.1 | Fabrication of Liquid Metal-Filled Through-Glass Vias

Glass-fiber reinforced polymer composite substrates with a thickness of 150 µm were used as the base material for LM-interposer fabrication. Arrays of TGVs with diameters ≥10 µm were drilled using a femtosecond laser system (Multifunction fs laser systems, UFL-300, L2K). To prevent LM residue from remaining on the substrate during the filling process, a shadow mask film patterned with via openings was attached to the substrate. A 2 µm-thick parylene-C layer was deposited on the glass (5x5 by chemical vapor deposition. Polydimethylsiloxane (PDMS) was then spin coated at 3000 rpm to form a 20 µm-thick film, which was subsequently cured and transferred onto the TGV surface. A shadow mask consisting of a 12 µm-thick polyimide (PI) film coated with Cr/Cu (5/100 nm) was prepared. The metal layers were patterned by photolithography using S1818 photoresist and wet etching in Au etchant (30 s) and Cr etchant (10 s), followed by photoresist removal. The patterned mask was aligned and attached to the PDMS layer. Reactive ion etching was performed using SF_6 (24 sccm) and O_2 (6 sccm) gases at 170 mTorr and 300 W for 40 min to open the via holes through the PDMS. The shadow mask film was then removed. A 5 mm-thick PDMS layer was attached to the bottom of the TGV substrate for mechanical support, and a 5 mm-thick EGaIn reservoir was applied to the top surface, covering the vias. The entire structure was placed in a vacuum chamber, and a VACI process was used to complete LM infiltration. Afterward, the PDMS layers were removed from both sides, yielding LM-filled TGV substrates.

After fabrication of the LM-filled TGV substrate, a Cr/Cu seed layer (10/200 nm) was deposited, and Cu electroplating was performed in cyclic voltammetry mode at a scan rate of 0.01 V s^{-1} for 15 min to form a 10 µm-thick Cu layer. S1818 was again applied and patterned to define the RDL traces, followed by immersion in a diluted Cu etchant for 80s to selectively remove unprotected Cu, forming the final Cu RDLs. After etching, the remaining photoresist was stripped, and the substrate was cleaned to complete the fabrication of the LM-interposer. A passivation layer was formed using SU-8 via standard photolithography. The chip was then precisely aligned to the interposer using a printing system. Bonding was performed either by direct LM 3D printing at the aligned position or by transferring a LM-ACA layer onto the chip surface before attaching it to the interposer. Finally, the completed LM-filled interposer was connected to the PCB using LM-ACA as the conductive adhesive.

4.2 | Glass-Fiber Substrate Preparation

A hybrid matrix resin was synthesized via a non-hydrolytic sol-gel reaction using 2-(3,4-epoxycyclohexyl)ethyltrimethoxysilane

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(ECTS) and diphenylsilanediol (DPSD) in a 1:1 molar ratio. The precursors were mechanically stirred, followed by the addition of barium hydroxide monohydrate ($Ba(OH)_2{\cdot}H_2O$, 0.1 mol%) as a base catalyst under nitrogen atmosphere at 80 °C for 5 hours, yielding a clear epoxy-functionalized siloxane hybrid (EPSH) resin. Subsequently, 20wt% of epoxy cross-linkable hardener (DOX, bis[1-Ethyl(3-oxetanyl)]methyl ether) and 1wt% of photo-initiator (triaylsulfonium hexafluoroantimonate salt) was added. To fabricate glass-fiber substrates, E-glass fabrics (25μm) were preheated on a OTS-treated glass plate at 80 °C. The EPSH resin was dispensed onto the glass fibers for thorough impregnation, and another OTS-treated cover glass plate was placed on top. The stacked layers were vacuum-pressed and cured under UV light (365 nm) for 3 minutes. The cured glass-fiber substrates were demolded from OTS-treated glass plates.

4.3 | Liquid Metal-Filled Cross-Sectional Imaging

The LM-filled vias were milled using an Aquilos 2 Cryo-FIB (Thermo Fisher Scientific, SNU CMCI), and the cross sections were imaged using a SEM.

4.4 | Calculation of AC Resistance in Liquid Metal-Filled via

Based on S-parameter measurements from a previous study on LMs, electrical conductivity and permittivity values were iteratively adjusted in simulations to fit the experimental graphs, enabling the extraction of the effective conductivity of the material [40]. Using frequency-dependent conductivity data for both Cu and EGaIn, the relaxation time constants were estimated via the Drude model, allowing the calculation of conductivity over the frequency range from 1 kHz to 10 GHz. CST simulations were performed for EGaIn using the same via structure as the referenced study. When a conductivity value of 3.4×10^6 S m^{-1} was assigned to EGaIn, the simulation results showed strong agreement with the reported data. From this, the relaxation time constant of EGaIn was determined to be ≈0.361 ns. Using the Drude model, the frequency-dependent conductivity of EGaIn was then computed over the 1 kHz to 10 GHz range. A similar approach was applied to Cu using parameters from the literature. For Cu with a thickness of 1 mm, the relaxation time constant was set to 0.039 ns, and the high-frequency conductivity was calculated accordingly [13]. Using these conductivity values, the frequency-dependent skin depth for both Cu and EGaIn was derived. To calculate the impedance and AC resistance of a cylindrical via (via radius: 300 μm, length: 100 μm), the skin effect was taken into account using the Bessel function-based model. This allowed for an accurate estimation of the AC resistance considering frequency-dependent current distribution within the conductor.

4.5 | Fabrication of 3D-Printed Liquid Metal Interconnects

To fabricate the printing nozzle, a glass capillary (Sutter Instrument; outer diameter: 1.0 mm, inner diameter: 0.5 mm) was thermally pulled using a micropipette puller (P-1000, Sutter Instrument), resulting in inner diameters ranging from 5 to 35 μm. The LM used for printing was EGaIn (eutectic gallium–indium; 75.5% gallium, 24.5% indium alloy by weight; Changsha Santech Materials Co. Ltd.). During the printing process, the nozzle's position was controlled using a six-axis stage (H-820 6-Axis Hexapod, Physik Instrument), and a microscope camera (QImaging Micropublisher 5.0 RTV, Teledyne Photometrics) was used to monitor the printing in real time. The syringe (used as the ink reservoir) was connected to the glass capillary nozzle and filled with EGaIn. EGaIn was then extruded through the nozzle using compressed dry air at 90 psi, which was applied prior to printing. During printing, a pressure in the range from 3 to 50 psi was applied depending on the nozzle diameter (5–35 μm).

4.6 | Electrical Characterization of Liquid Metal

Impedance measurements were carried out using a multichannel potentiostat (PMC-1000, AMETEK) over a frequency range from 1 Hz to 1 MHz. Two metal contact pads, spaced 300 μm apart and composed of Cr (5 nm), Au (500 nm), and Pt (60 nm), were connected using EGaIn 3D printed with a diameter of 20 μm. Subsequently, a four-point probe setup was employed to measure the current through the LM under an AC bias (120 Hz) applied by a SourceMeter (2400 Series SMU, Keithley), using a probe station (Keithley 4200-SCS).

4.7 | Mechanical Reliability Tests

For the bending test, cyclic deformation was applied using a stretching stage by moving the stage perpendicular to the LM interconnect over a displacement of 150 μm for 1,000 cycles. For the vibration fatigue test, the sample was subjected to vibration loading at 175 Hz with an acceleration of 1.5 Grms for 1,000 min.

4.8 | Thermal Characterization of 3D-Printed LM Interconnects

For thermal characterization, the 3D-printed LM interconnect was electrically biased using a SourceMeter (2400 Series SMU, Keithley), while the voltage was monitored simultaneously. The temperature distribution was measured by long-wave infrared thermography using an IR camera (T650sc, FLIR Systems, Wilsonville, OR, USA). Thermal images were recorded under increasing input power, and the maximum temperature rise of the freestanding LM interconnect was extracted from the corresponding thermal maps.

4.9 | Liquid Metal-based Anisotropic Conductive Adhesive

To fabricate the LM-ACA, SIS, toluene, quintone, and EGaIn were combined in a 10 mL vial at a weight ratio of 1:9:0.3:5-80, targeting applications such as chip-to-interposer and interposer-to-PCB bonding. The blend was subjected to ultrasonication at 130 W (40% amplitude) for 1 h to disperse the EGaIn into fine particles. The resulting dispersion was spin coated onto release paper at 3000 rpm for 40 s. After thermal curing, the adhesive

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film was transferred onto both the chip and interposer, and a bonding force exceeding 60 N was applied using a Mark-10 force gauge to ensure proper adhesion.

4.10 | Liquid Metal-Interposer Operation Demonstration at System Level

An LM-filled TGV interposer was used to integrate the processor and sensor chips, which were then mounted on a PCB [39, 41]. These chips had previously been used in a millimeter-scale sensing system platform, in which multiple chiplets are vertically stacked to minimize system volume and enable a chiplet-based modular design [41, 42]. The system-level demonstration setup using the interposer system was configured as follows. A laptop controlled a system programming board via USB, which programmed the processor chip on the interposer system using a single-wire protocol [43]. The processor chip controlled the sensor chip to perform temperature measurements and output the data over four wires for chip-to-chip communication following a bus protocol [38]. The four wires were CIN (clock input), COUT (clock output), DIN (data input), and DOUT (data output). Among these, the COUT and DOUT signals were buffered by discrete amplifiers on the PCB. A logic analyzer (Saleae), together with a laptop, was used to read out and interpret the measured temperature data from these signals. The integrated system was supplied with 3.3, 1.3, 0.7, and 5.0 V. The first three supplies powered the processor and sensor chips, while the 5 V supply powered the discrete amplifiers. All grounds of the two chips, power supplies, and logic analyzer were connected to the building earth ground. Some of the power supplies were replaced with a SourceMeter (2400 Series SMU, Keithley) to measure current consumption while providing the same voltage.

System-level operation was demonstrated by programming the processor chip with C code to perform periodic temperature measurements through the system programming board. The integrated system output temperature data, which were captured by the logic analyzer and its supporting software on the laptop and saved as a text file with time stamps. To evaluate the accuracy of the temperature measurements, an IR camera (T650sc, FLIR Systems, Wilsonville, OR, USA) oriented normal to the die surface was used as a reference. The binary temperature data obtained from the integrated system were converted to °C using a two-point calibration at 27.4°C and 40.8°C based on the IR camera measurements. A temperature-versus-time plot was then generated by applying the calibration equation to all binary temperature data collected over time.

Author Contributions

Inhea Jeong and **Wonjung Park** contributed to ideation and carried out experiments, analyzed the data, and wrote the manuscript. **Won Gi Chung**, **Min Gyo Jeong**, and **Seung Hyun An** performed LM-filled TGV fabrication. **Heungsik Eum** and **Ehab A. Hamed** contributed to the system-level demonstrations. **Hyun Seok Kang** fabricated the glass-fiber substrates. **Dong Wook Park** calculated the skin depth and frequency-dependent AC resistance of EGaIn. **Jeong Min Woo** oversaw the high-frequency AC-resistance characterization of EGaIn. **Byeong-Soo Bae** oversaw experiments involving the glass-fiber substrates. **Inhee Lee** oversaw the system-level demonstrations and revised the manuscript. **Jang-Ung Park** supervised all phases of the research and revised the manuscript. All authors discussed the results and reviewed the manuscript.

Acknowledgments

This work was supported by the Ministry of Science & ICT (MSIT), the Ministry of Trade, Industry and Energy (MOTIE), the Ministry of Health & Welfare, and the Ministry of Food and Drug Safety of Korea through the National Research Foundation (RS-2023-NR077138, RS-2025-18362970, RS-2025-16063568), STEAM Research Programs (RS-2024-00460364), Technology Innovation Program (RS-2025-08672969), ERC Program (RS-2024-00406240), and Korea Institute of Science and Technology (KIST) Institutional Program (2E33191 and 2E33190). The authors thank the financial support by the Institute for Basic Science (IBS-R026-D1).

Funding

This study was supported by National Research Foundation of Korea (Grant RS-2023-NR077138, RS-2025-08672969, RS-2024-00460364, RS-2025-16063568, and RS-2025-18362970), Ministry of Science and ICT, South Korea (Grant RS-2024-00406240), Korea Institute of Science and Technology (Grant 2E33191, and 2E33190), and Institute for Basic Science (Grant IBS-R026-D1).

Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Additional SI can be found online in the Supporting Information section.

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